Design Name : Use of RAM primitive from Xilinx library

Objective :

Learn how to incorporate Block RAMs (of Spartan-3E) in VHDL designs.

Assignment :

Spartan-3E, line many other FPGAs, includes several block RAMs that can be used in designs with the help of UNISIM library.

1. Select *Language Templates* ( ) from *Edit* menu. (or from toolbar, if exists). Language Templates list will appear in a tabulated window.
2. From the template tree select *Device Primitive Instantiation –> FPGA –> RAM / ROM –> Block RAM –> Spartan 3E –> Single Port -> RAMB16_S9*
3. Copy the template from the right portion of the split-window into your code (architecture section, after begin)

Now, a block RAM of 2kB is ready to be used in your designs. You may change the instantiation name to any allowable string.
The operation timing diagram of the block RAM is given in the figure below which is copied from Spartan-3E Generation FPGA User Guide.

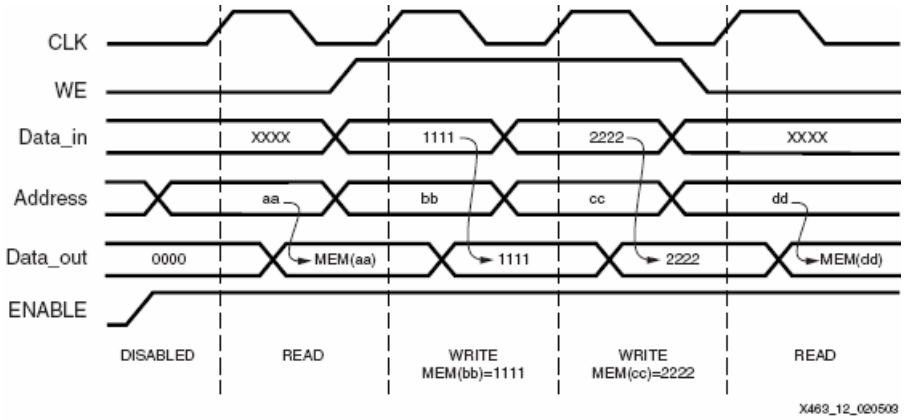

Figure 4-12: **WRITE_FIRST Mode Waveforms**

4. Put your own INIT values into BRAM instantiation, Design a circuit that brings up the RAM bytes one-by-one in every 0.5 seconds and feed the LEDs with these values. You may bring up the design you did in previous lab session (*9 Another State Machine*). Limit the address counter to the end of your initialized bytes.

Follow Up Work :

Obtain a 4kB BRAM using two 4Kx4 BRAMs (RAMB16_S4)

Homework :

Let the parity bit indicate the end of sequence. When a '1' is seen in parity bit, retrieve next start address from another BRAM. Second BRAM has a number of starting addresses of sequences. The design will be like shown in the following figure

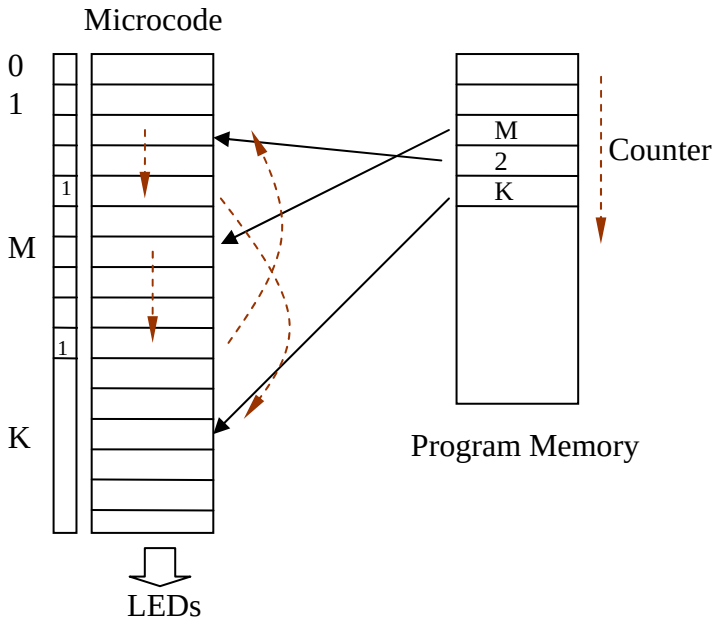

Figure 2. RAM usage in design.