Design Name : Inference and Use of RAM Blocks

Objective :

Learn how to incorporate Block RAMs (of Spartan-3E) in VHDL designs.

Some Info :

Spartan-3E, like many other FPGAs, includes several Distributed and Block RAMs that can be used in designs with the help of UNISIM library. The type definition

```
type TDPRAM is array (0 to 127) of std_logic_vector (7 downto 0);
```

defines a RAM as a register set of size 128 and width of 8 and the signal declaration

```
signal MRAM : TDPRAM;
```

instantiates such a RAM. Now, a RAM of 128 Bytes is ready to be used in your designs. Realization of the MRAM depends on the use/access to its elements. If many elements are accessed simultaneously discrete FFs are used. Otherwise, if the size is less than the sizes of Distributed RAMs, then Distributed RAMs are used. If the size is too large to fit in Distributed RAMs, then Block RAMs are used, provided that simultaneous addressing to multiple elements can be established by the embedded Block RAMs. For example; Spartan-3E has 2Kbytes Block RAMs with dual address ports. Therefore, a design that access simultaneously 3 addresses cannot be realized. However, if the size is less than 10Bytes for example, this can be realized with discrete FFs. Synthesis and implementation depends on the FPGA selected in the project.

Assignment :

1. Define a RAM with 100 Bytes. Place x"11", x"22", x"44", x"88", x"FF" values on it. Write process that sends these values on LEDS in 0.5s intervals consecutively, starting from the beginning after the last value.
2. Change your design to start from beginning only when x"01" is encountered.

Follow Up Work :

3. Declare a 1 K x 16 RAM and see if it works.
4. Write a process that access to 3 consecutive words from this RAM. Test to see if it works.
5. Declare a 4 KB RAM and see if it works (Do not forget to use UNISIM library declaration)

Homework :

6. Redesign the circuit at assignment-1 using 2KB memory. This time increment the value at the memory position just read.