Design Name : A 3 to 8 Decoder with Invert Input

Objective :

Learn WITH-SELECT-WHEN concurrent statement in combinatorial circuits.

Assignment :

1. A circuit with the following truth table is to be implemented. SWS and Invert are 3 and 1 bit inputs respectively whereas LEDS is an 8 bit output,

Invert	SWS	LEDS	Invert	SWS	LEDS
0	000	00000001	1	000	11111110
0	001	00000010	1	001	11111101
0	010	00000100	1	010	11111011
0	011	00001000	1	011	11110111
0	100	00010000	1	100	11101111
0	101	00100000	1	101	11011111
0	110	01000000	1	110	10111111
0	111	10000000	1	111	01111111

- 2. Use WITH-SELECT-WHEN to assign appropriate value to the output LEDS.
- 3. Synthesize your design. Correct if there are errors.
- 4. Examine RTL-schematics to see if it matches your expectation. Draw RTL schematic in your report.
- 5. Complete the constraints file by connecting Invert and SWS inputs to switches on FPGA kit. Connect LEDS output to on board LEDs.
- 6. Implement your design and build binary programming file.
- 7. Power-up and program your FPGA device through USB cable connection. Check if your design works as desired.
- 8. Analyze synthesis report and see the resource usage percentages. Put your resource usage (the number of FFs, gates and other stuff) in your report.

Questionary :

If you had a chance to design your circuit manually instead of using VHDL what would you change in the circuit? Why? Type your answer in your report.

Follow Up Work :

Change your design and use WHEN-ELSEs. Check RTL-schematics see if there are any changes. Type in your comments in the report.

Homework :

Add another input to your design. Connect it to one of the push-buttons (South). Let this button reverse the bit order of the output, that is LSB is represented by leftmost LED and MSB is represented by rightmost one.

