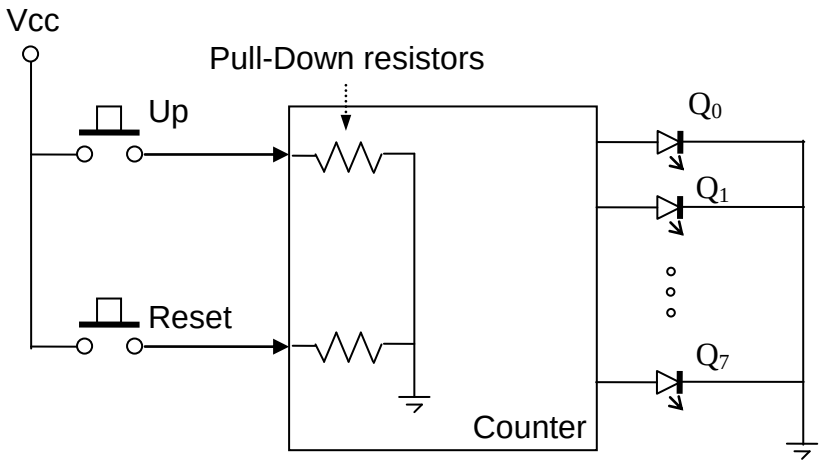
Design Name : Up Counter With Asynchronous Reset, Simulation

Objective :

Learn asynchronous primitive circuit description and implement it on the FPGA kits for practice. Also start using ISIM simulator.

Assignment :

1. Describe an 8-bit binary counter with Up and Reset inputs as shown in the figure.
2. Connect inputs to push buttons of your choice on the FPGA kit. Do not forget internal pull-down resistors as a design constraint. Connect outputs of the counter to LEDs on the FPGA kit. They already have current limiting resistors in serial (not shown here).
3. Power-up and program your FPGA device through USB cable connection. Check if your design works as desired.



4. If the design does not operate as expected, go back to your VHDL code and analyze. Correct design problems and re-test. Examine RTL-schematics. Put your RTL schematic into your report.

Follow Up Work :

1. Redesign your counter to have a synchronous-Reset instead of an asynchronous one. Compare the two for their possible advantages-disadvantages. Type your comments in your report.
2. Simulate your circuit. Stimulate with at least two reset pulses to conclude that your circuit surely works as expected.

Questionary :

Did your counter increment multiple times sometimes although you pressed the increment button only once? How do you think you can resolve this problem? Put your answer into the report.

Homework :

Design an Up-Down counter with one clock input, one Up/Dwn direction input and one asynchronous-Reset input.