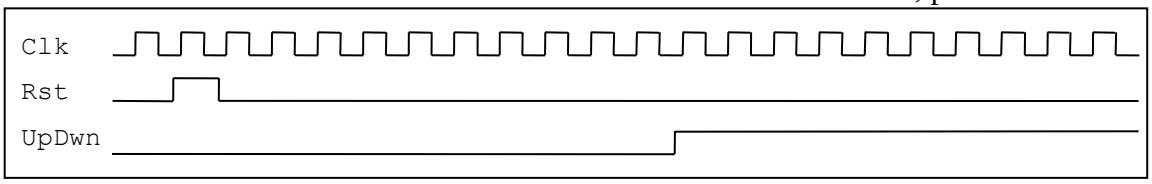
Design Name : Waveform Simulation of an Up-Down Counter

Objective :

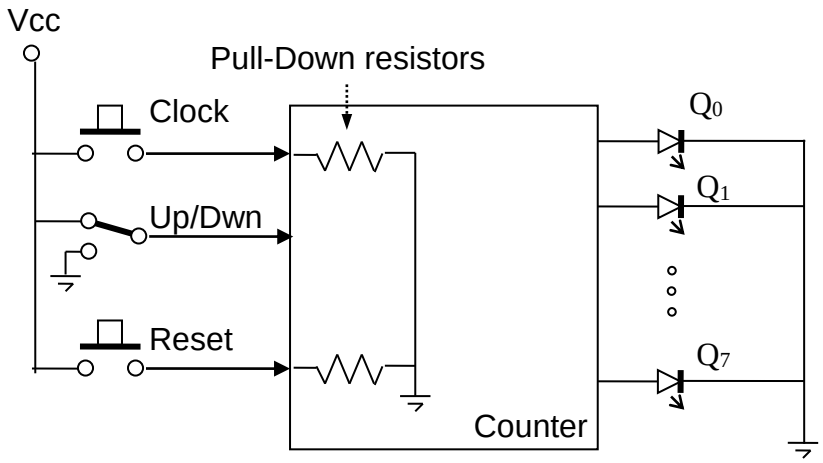
Learn how to simulate the behavior of an up-down counter. Learn how to generate waveform and VHDL stimulus for simulation. .

Assignment :

1. Describe an 8-bit binary counter with Clock, Up/Dwn and synchronous Reset inputs as shown in the figure.
2. Select Simulation (not Implementation) radio button on the top of the project tree. Create a new VHDL Test Bench using File-New.
3. Create stimulus waveforms as shown. `Clk` durations are both 10 ns, period is 20 ns.



4. Check testbench syntax and start simulation. Display counter output as decimal numbers. Does it behave as you expected? If not, correct your design. Put the resulting waveform into your report.
5. Display output in binary format. Put your binary waveforms into the report.
6. Connect Clk and Reset inputs to push buttons of your choice on the FPGA kit. Do not forget internal pull-down resistors as a design constraint. Also, connect Up/Dwn input to a two-position switch as illustrated.
7. Connect outputs of the counter to LEDs on the FPGA kit. They already have current limiting resistors in serial (not shown here).
8. Power-up and program your FPGA device through USB cable connection. Check if your design works as you expected.



Questionary :

What do you think of simulation? Does it help to pinpoint design errors?

Homework :

Change your clock to have asymmetric duty cycles in your test bench (and report).