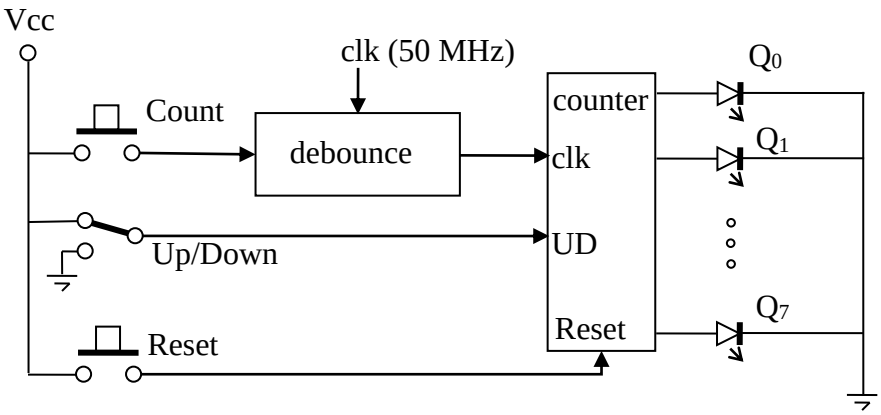
Design Name : Key Debouncer

Objective :

Understand the bouncing on mechanical switches. Learn how to eliminate this effect and obtain clear transitions.

Assignment :

1. Describe an 8-bit binary counter with Clock, Up/Dwn and synchronous Reset inputs as shown in the figure. This work has been previously done in experiment named "3b Up-Down Counter Sim". So you may copy entire project or just VHDL codes from it. Make it work before continuing. The counter might increment/decrement multiple counts when a button is pressed. That is okay, now we will fix this behavior.
2. Create a new VHDL module and name it as "debounce.vhd". Type in your debouncer design and create debounce entity. You should have had created it as a homework and brought it into the lab.



3. Using the debounce entity as a component, debounce the Count key input. If your design is correct, multiple increment/decrement phenomena will be eliminated. In your report, explain why other inputs (Up/down and Reset) need not be debounced.

Questionary :

How did you decide on the value of the debouncing delay? How many samples did you capture from the key? Why?

Homework :

1. Now that clk input of the counter is just an ordinary signal, consider detecting transitions of it using 50MHz clock signal as a clock. What would you do to achieve that?
2. Let us assume that debouncing sample period is 5 ms and you are using a counter to generate sampling pulses from a 50 MHz clk input. What would be the advantage of moving this counter out of the debounce block and input a 1000/5=200 Hz sampling clock to this debounce block?