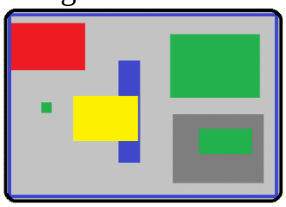
Introduction to VHDL-FPGA 2022-Fall
FPGA / VHDL Term Projects

1. VGA with Selectable Resolution

Group 1: (?,?)

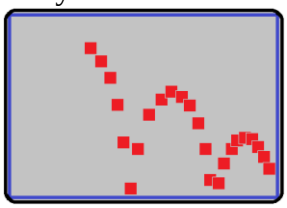
A connected VGA monitor will be put in one of at least 3 preset resolutions. N rectangles with random size/color will appear on it in selectable rate and will stay there until their properties change.



2. Gravity

Group 2: (?,?)

On a VGA screen, objects with selectable stiffness will appear randomly and start bouncing under a selectable gravity until they move off the visible area. It will repeat the this action at every 3 seconds with random changes of color, stiffness and gravity.



3. Simple Microprocessor/Controller

Group 3: (?,?)

An 8-bit microprocessor/controller and its instruction set will be designed. Instruction set, at minimum, will consist of arithmetical (ADD, SUB), logical (AND, OR, NOT, XOR), flow (JMP, JIF, JSR, RET), transfer (IN, OUT) instructions and their variations. It might have additional local registers including flags for the last instruction. A simple demonstration that uses most of the instructions is necessary.

```
EXAMPLE2: MOV  DPTR,#50H
          MOV  R7,#0
REPEAT:   MOVX A,@DPTR
          INC  DPTR
IF:       CJNE A,#'0',$+3
          JC   UNTIL
          CJNE A,#'9'+1,$+3
          JNC  UNTIL
THEN:     INC  R7
UNTIL:    CJNE A,#0,REPEAT
          MOV  A,R7
HERE:     SJMP HERE
          END
```

Not: Use of a predesigned processor/controller is prohibited.

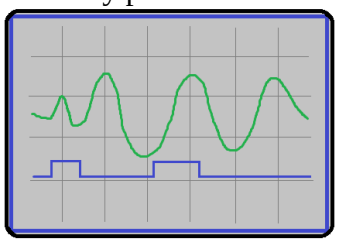
4. Simple Scope

Group 4: (?,?)

Voltage seen at the ADC input will be displayed on the VGA screen graphically and continually. It will act like a low bandwidth small signal oscilloscope. The following will be considered for grading;

1. Trigger function (from input or external)
2. Number of channels
3. Having digital inputs
4. Input gain adjustment
5. Scan frequency adjustment (sample rate?)
6. On-screen cursor and text (axis values, for example)

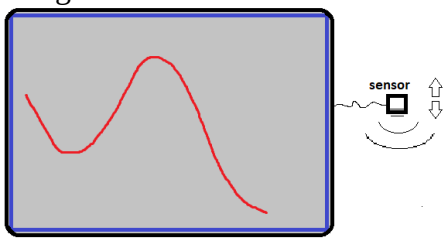
You may prefer to use on-board ADC or use an external ADC module.



5. Ultrasound Range Finder

Group 5: (?,?)

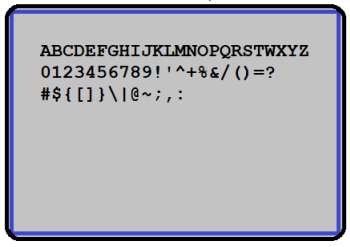
An ultrasound detector will measure the distance from the floor. In calibration mode, it will record the distance from the floor and use it as the largest distance. In operation mode, it will continuously measure the distance and display it as a graphic on VGA screen, the last point being the last measurement.



6. Character Generator

Group 6: (?,?)

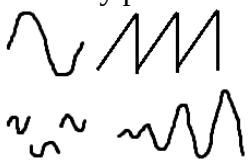
Character generator is a circuit that translates ASCII characters in a memory block to their bitmap symbols for displaying characters on a display device (e.g. VGA monitor). For simplicity, let each symbol is a 8x8 bitmap of 0s and 1s. Your circuit will read ASCII characters from one memory block and generate the signal required to display the bitmap on VGA, which must be synchronous with the VGA signals (HSYNC, VSYNC and pixel coordinates). Have variable width character capability for bonus points. Have color capability (given along with the ASCII character) for bonus points.



7. Signal Generator

Group 7: (?,?)

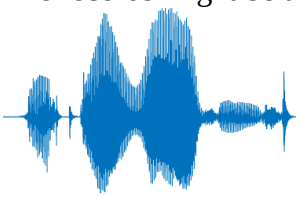
An arbitrary signal generator will be designed. Signal shape can be selected from pre-defined patterns or user defined. It basically plays out signal samples that are stored in a memory block and converts this digital signal to analog. Frequency should be adjustable. Amplitude can be selected from multiple pre-defined amplitudes. Predefined shapes can be sine-wave, staircase, triangular, saw-tooth etc. Have multiple synchronous signal outputs for bonus points. Have the signals displayed on a VGA display for bonus points.
You may prefer to use on-board DAC or use an external DAC module.



8. Voice Synthesizer

Group 8: (?,?)

Two short voice records (waveform file, .wav) will be played out through DAC and will be heard from the amplified speaker. Two buttons will be used to select one of the records from memory. The records might be the waveforms of the spoken words like "one" and "zero".



9. IR Tranceiver

Group 9: (?,?)

A serial transmission protocol will be used to transmit data through IR to another FPGA board. May use loop-back or mirror to employ single FPGA board. IR or visible light LEDs will be needed.

Note: Projects completely harvested from the internet will be considered as ***plagiarism***.
Difficulty of the project, documentation, presentation and demonstration are to be **considered in grading**.
Grading: 0.3xD+0.5xW+0.1xP+0.1xE
D:Difficulty, W:WorkingDemo, P:Presentation, E:ExtrasPutInProjectByGroup.

The tentative schedule is;
January 2nd 2022, Monday : Online presentation of the projects. Last day for sending in the documentation and closing up the projects.

Documentation is (all soft):

1. Presentation video (max 20 minutes).
2. 5-10 pages of project report not including titles, codes and large schematics.
    a. Include pictures, schematics (descriptive block diagrams are very important)
    b. Use scientific paper (or white paper) format and rules (very important!)

3. Project directory including VHDL codes (all in a single *.rar file). Clean up the project before handing in (`Project->Cleanup` in ISE or `reset_project` in TCL console in Vivado).