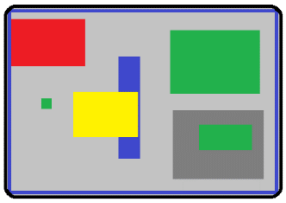
Introduction to VHDL-FPGA 2023-Fall
FPGA / VHDL Term Projects

1. VGA with Selectable Resolution

Group 1: (?,?)

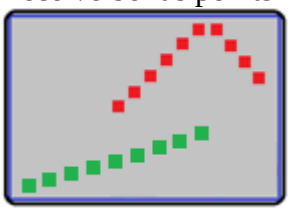
A connected VGA monitor will be put in one of at least 3 switch-selected resolutions. N rectangles with random size/color will appear on it in selectable rate and will stay there until their properties change. N should be between 10 and 100. Resolution change will affect the sizes and coordinates of new rectangles. A rectangle will stay on the screen for a random duration between 0.1s and 2s. Receive bonus points for additional resolutions.



2. Bouncing

Group 2: (?,?)

On a VGA screen, N objects with random color and initial direction will appear at the center and start bouncing between edges of the screen. Objects will appear at 1s intervals until N is reached. Receive bonus points for adjustable object speed.



3. Picoblaze

Group 3: (?,?)

Two Picoblaze microcontrollers will be used for Tx and Rx ends of a serial communication. Tx end will read switches continuously and transmits through J1 general purpose header. Rx end will display received data from J2 header on LEDs continuously. Receive bonus points for asynchronous tranceiver.

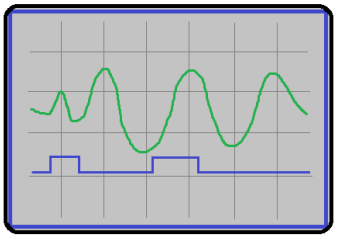
4. Simple Scope

Group 4: (?,?)

Voltage seen at the two on-board ADC inputs will be displayed on the VGA screen graphically and continually. It will act like a two channel low bandwidth small signal oscilloscope. The following will be considered for grading;

1. Trigger function (from input or external)
2. Having digital inputs
3. Input gain adjustment
4. Scan frequency adjustment (sample rate?)

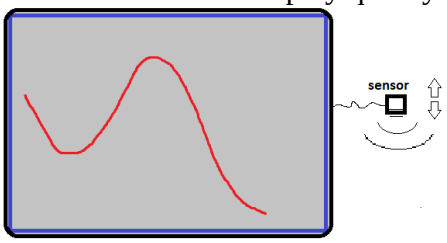
You may prefer to use on-board ADC chip or use an external ADC module.



5. Servomotor Control

Group 5: (?,?)

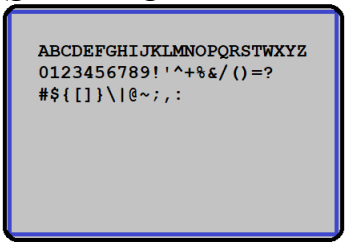
Two servomotors will be controlled by the input devices (buttons, switches, rotary) on the board. Two target angles will be displayed on a VGA screen. Receive bonus points for homing limit-switches and VGA display quality/intuition/creativity.



6. Character Generator

Group 6: (?,?)

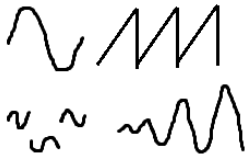
Character generator is a circuit that translates ASCII characters in a memory block to their bitmap symbols for displaying characters on a display device (e.g. VGA monitor). For simplicity, let each symbol is an 8x8 bitmap of 0s and 1s. Your circuit will read ASCII characters from one memory block and generate the signal required to display the bitmap on VGA, which must be synchronous with the VGA signals (HSYNC, VSYNC and pixel coordinates). Have variable width character capability for bonus points. Have color capability (given along with the ASCII character) for bonus points.



7. Signal Generator

Group 7: (?,?)

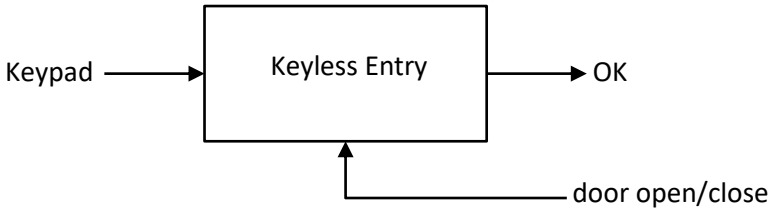
An arbitrary signal generator will be designed. Signal shape can be selected from pre-defined patterns or user defined. It basically plays out signal samples that are stored in a memory block and converts this digital signal to analog. Frequency should be adjustable. Amplitude can be selected from multiple pre-defined amplitudes. Predefined shapes can be sine-wave, staircase, triangular, saw-tooth etc. Have multiple synchronous signal outputs for bonus points. Have the signals displayed on a VGA display for bonus points.
You may prefer to use on-board DAC or use an external DAC module.



8. Keyless Entry

Group 8: (?,?)

A 10 key keypad will be used to enter 6 digit codes. When the correct code is entered, OK signal is generated for 10 seconds in which a door open signal is expected to be received. When door is closed device will enter into Lock mode. A Set-mode should exist for setting a new code. A logical-flow design is expected, not just a code entry circuit. Receive bonus points for additional alarms, door control outputs etc.



9. IR Tranceiver

Group 9: (?,?)

A serial transmission protocol will be used to transmit data through IR to another FPGA board. May use loop-back or mirror to employ single FPGA board. IR or visible light LEDs will be needed. Member must find a way to display the received data. Receive bonus points for receiving from an existing remote control device.

Note: Projects completely harvested from the internet will be considered as ***plagiarism***. Difficulty of the project, documentation, presentation and demonstration are to be **considered in grading**.

Grading: 0.3xD+0.5xW+0.1xP+0.1xE

D:Difficulty, W:WorkingDemo, P:Presentation, E:ExtrasPutInProjectByGroup.

The tentative schedule is;

January 11th 2023, Thursday : Online presentation of the projects. Last day for sending in the documentation and closing up the projects.

Documentation is (all soft):

1. 5-10 pages of project report not including titles, codes and large schematics.
    a. Include pictures, schematics (descriptive block diagrams are very important)
    b. Use scientific paper (or white paper) format and rules (very important!)
2. Project directory including VHDL codes (all in a single *.rar file). Clean up the project before handing in (`Project->Cleanup` in ISE or `reset_project` in TCL console in Vivado).
3. Presentation pptx file.