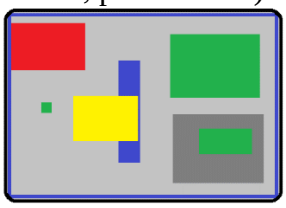
Introduction to VHDL-FPGA 2025-Fall
FPGA / VHDL Term Projects

Note: Instructor will demonstrate; VGA signal generation, Pseudo-random number generation within a few weeks.

1. VGA with Selectable Resolution

Group 1: (?,?)

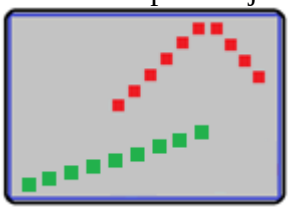
A connected VGA monitor will be put in one of at least 3 switch-selected resolutions. Parameters of the selected resolution will be stored in an array of records and one of them will be selected via switches or rotary. Additional parameter sets can be added to the record array for different resolutions. Selectable (via switches of rotary) number (between 10 and 50) of rectangles will appear on the screen with pseudo-random positions/sizes/colors. At every 0.1s a random of the rectangles will change its properties. Receive bonus points for additional shapes (like triangles, circles, patterns etc.).



2. Bouncing Objects

Group 2: (?,?)

On a VGA screen, N objects (N between 10 to 20) with random color, position, initial direction and speed will appear at the center and start bouncing between the edges of the screen. Object parameters (position, speed, heading, color etc.) will be kept in an array of records. All N objects will be seen bouncing on the screen. Initial object speeds will be random within some acceptable (visually trackable) range. Objects can be small rectanges in a simplest design. Receive bonus points for objects with different shapes(like triangles, circles, patterns etc.). Receive bonus points for rotary adjusted speed (all objects with same percentage change at the same time, not individual speed adjustment).



3. Picoblaze

Group 3: (?,?)

This one is exacly like the project Bouncing Objects but done using Picoblaze microcontroller, except the VGA signal generation which will be designed in VHDL.

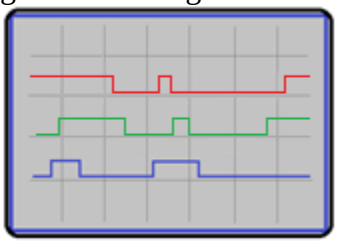
4. Simple Binary Scope

Group 4: (?,?)

16+ binary inputs will be displayed on a VGA screen like an oscilloscope/logic analyzer. The following are required;

1. Trigger function (from input or external or one shot)
2. Scan frequency adjustment (sample rate?)
3. Hold (keep what is displayed)

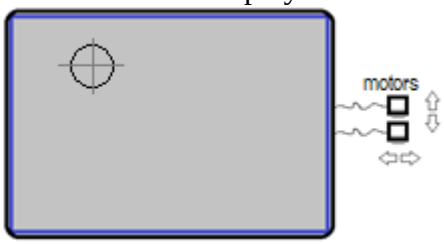
You may start developing scope functions using internally generated signals (placed in RAM, or generated using counters etc.).



5. Servomotor Control

Group 5: (?,?)

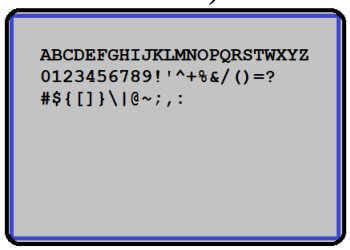
Two servomotors (driven by PWM) will be controlled by the input devices (buttons, switches, rotary) on the board. A mechanical design (or use of a pre-designed system) for controlling and directing a laser-pointer to a target is required. Receive bonus points for homing limit-switches and some VGA display functions.



6. Character Generator

Group 6: (?,?)

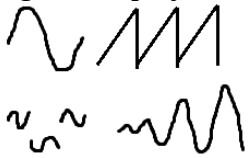
Character generator is a circuit that translates ASCII characters in a memory block to their bitmap symbols for displaying characters on a display device (e.g. VGA monitor). For simplicity, let each symbol is an 8x8 bitmap of 0s and 1s. Your circuit will read ASCII characters from one memory block and generate the signal required to display the bitmap on VGA, which must be synchronous with the VGA signals (HSYNC, VSYNC and pixel coordinates). Have variable width character capability, color capability (given along with the ASCII character) for bonus points.



7. Signal Generator

Group 7: (?,?)

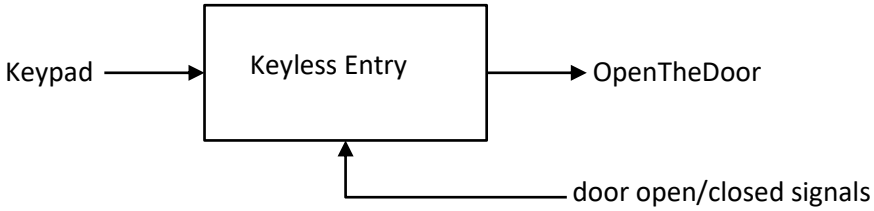
An arbitrary signal generator DDS will be designed. Signal shape can be selected from pre-defined patterns or user defined. It basically plays out signal samples that are stored in a memory block and converts this digital signal to analog through on-board DACs (or external DAC modules). Frequency should be adjustable. Predefined shapes can be sine-wave, staircase, triangular, saw-tooth etc. Have multiple synchronous signal outputs for bonus points. Have the signals displayed on a VGA display for bonus points.



8. Keyless Entry

Group 8: (?,?)

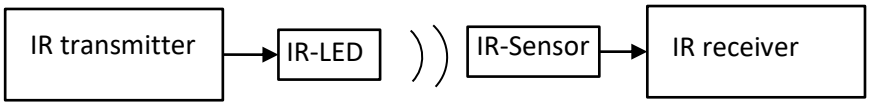
A 10 key keypad will be used to enter N digit codes. When the correct code is entered an `OpenTheDoor` signal is generated for 2 seconds. A `DoorOpen` signal is expected to be received afterwards (a sensor is needed). When door is closed by the entree, device will enter into Lock mode, clearing entered code. A Set-mode should exist for setting a new code. A logical-flow design is expected, not just a code entry circuit. Receive bonus points for additional alarms like `doorleftopen`, door control outputs like `turnonlights`, `buzzeron` signal when code is entered incorrectly 5 consecutive times etc.



9. IR Tranceiver

Group 9: (?,?)

A serial transmission protocol will be used to transmit data through IR to another FPGA board. May use loop-back (and mirror) to employ single FPGA board. IR or visible light LEDs will be needed. Designers must find a way to display the received data. Receive bonus points for receiving from an existing remote control device (TV remote maybe).



Note: Projects completely harvested from the internet will be considered as ***plagiarism***.
Difficulty of the project, documentation, presentation and demonstration are to be **considered in grading**.
Grading: 0.3xD+0.5xW+0.1xP+0.1xE
D:Difficulty, W:WorkingDemo, P:Presentation, E:ExtrasPutInProjectByGroup.

The tentative schedule is;
December 30th 2025, Tuesday : In-class presentation of the projects. Last day for sending in the documentation (to eseke@ogu.edu.tr) and closing up the projects.

Documentation is (all soft):

1. 5-10 pages of project report not including titles, codes and large schematics.
    a. Include pictures, schematics (descriptive block diagrams are very important)
    b. Use scientific paper (or white paper) format and rules (very important!)
2. Presentation pptx file.
3. Project directory including VHDL codes (all in a single *.rar file). Clean up the project before handing in (`Project->Cleanup` in ISE or `reset_project` in TCL console in Vivado).

All documentation must have Numbers&Names of the group members in the first page.