No : Answers **Name : Solutions**

Eskişehir Osmangazi University Faculty of Engineering and Architecture

Department of Computer Engineering 16.11.2016

"*Introduction To VHDL*" Midterm Exam.

Note : Books, notes, computers are allowed, communication of all kind is prohibited. 90 (ninety) minutes.

1. When button `btn` is pressed, output `A` goes high for 2 seconds. When `A` goes low, output `B` is set to high for 1 seconds, then it goes low too. `btn` has no effect until this sequence completes. System operates on a 1 MHz `clk` input. Design the circuit using VHDL.

```
entity MYSEQ is Port (
   btn  : in  STD_LOGIC;
   A, B : out STD_LOGIC;
   clk  : in  STD_LOGIC); -- 1 MHz
end MYSEQ;

architecture MYSEQ of MYSEQ is
  signal tmr : integer;
  signal seq : STD_LOGIC;
begin

  process(clk) is begin
    if(rising_edge(clk)) then
      if(btn='1') then
        seq <= '1';
      end if;
      if(seq='1') then
        if(tmr=0) then
          A <= '1';
        elsif(tmr=2000000) then -- 2 seconds
          A <= '0'; B <= '1';
        elsif(tmr=3000000) then -- 3 seconds
          B <= '0'; seq <= '0';
        end if;
        if(tmr=3000000) then
          tmr <= 0;
        else
          tmr <= tmr+1;
        end if;
      end if;
    end if;
  end process;

end MYSEQ;
```

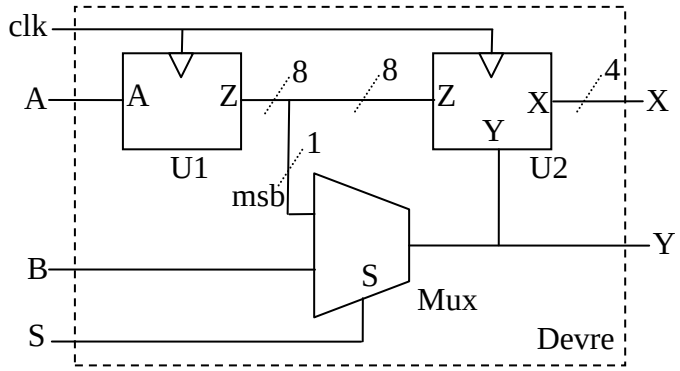
2. Design a 16 bit serializer (parallel to serial converter) using a shift register. Parallel data comes in through `P` port and serial bits come out from `S` port at each clock pulse. After each 16 bits sent, new 16 bit data is loaded at the same time again and its LSB is immediately seen at the output. Use as minimum amount of code as you can.

```
entity P2S is Port (
  clk : in  STD_LOGIC;
  P   : in  STD_LOGIC_VECTOR(15 downto 0);
  S   : out STD_LOGIC);
end PS2;

architecture P2S of P2S is
  signal SR   : STD_LOGIC_VECTOR(15 downto 0);
  signal cntr : STD_LOGIC_VECTOR(3 downto 0);
begin

  process(clk) is begin
    if(rising_edge(clk)) then
      if(cntr="0000") then
        SR <= P;
      else
        for i in 0 to 14 loop
          SR(i) <= SR(i+1);
        end loop;
      end if;
      cntr <= cntr+1; -- overflows at 1111 to 0000
    end if;
  end process;
  S <= SR(0);
end P2S
```

3. Assuming that the related components, U1 and U2, are declared appropriately, complete the top-level VHDL circuit according to the given block diagram. You need to add proper code for the 2-input 1-bit multiplexer and declare local signals too.




```
entity Devre is port (
  clk : in  STD_LOGIC;
  B, S: in  STD_LOGIC;
  A   : in  STD_LOGIC_VECTOR(7 downto 0);
  X   : out STD_LOGIC_VECTOR(3 downto 0);
  Y   : out STD_LOGIC);
end Devre;

architecture Devre of Devre is
  -- assume that components are already here
  signal Z : STD_LOGIC_VECTOR(7 downto 0);
  signal L : STD_LOGIC;
begin

  U1i: U1 port map(
    clk => clk,
    A   => A,
    Z   => Z
  );

  L <= (S and B) or (not(S) and Z(7));

  U2i: U2 port map(
    clk => clk,
    Z   => Z,
    Y   => L,
    X   => X
  );

end Devre;
```