No : **Name :**

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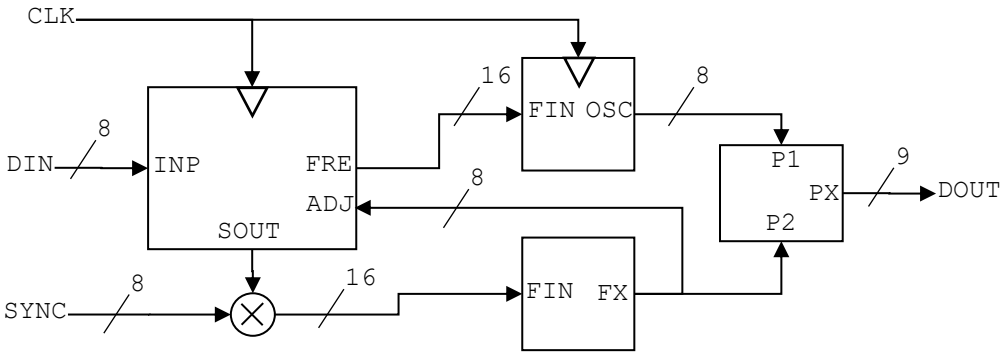
"*Introduction To VHDL-FPGA*" 1st Midterm Exam. 28.11.2020

1. The following obfuscated VHDL code with some syntax error(s) is given. You are expected to make the code readible by applying the following rules and then correct the syntactic errors.
   - sub-elements/statements are indented by 2 space characters
   - new statements/declarations are on separate lines
   - keywords:blue, functions:purple, comments:gray, literals:green, others:black
   - usage of upper/lower case is consistent throughout the code. All words (keyword or not) will have the same case with their first appearance in the code. Do not change the first appearance.

```
entity BCDcounter is Generic(Ndigits:in integer:=3);Port(UPDWN:in
STD_LOGIC;CLK:in STD_LOGIC;RESET:in STD_LOGIC;Q:out
STD_LOGIC_VECTOR(4*Ndigits-1 downto 0));end
BCDcounter;architecture BEHAV of BCDcounter is signal
CNT:STD_LOGIC_VECTOR(4*Ndigits-1 downto 0):=(others=>'0');begin
Q<=CNT;CX:for i in 0 to Ndigits-1 generate
process(clk,CNT,RESET,UPDWN)is begin if(RESET='1') then CNT(i*4+3
downto i*4)<=(others=>'0');elsif(rising_edge(clk)) then
if(UPDWN='0')then if(CNT(i*4+3 downto i*4)="1001")then CNT(i*4+3
downto i*4)<="0000";elsif(((i>0)and(CNT((i-1)*4+3 downto (i-
1)*4)="1001"))or(i=0))then CNT(i*4+3 downto i*4)<=CNT(i*4+3
downto i*4)+1;end if;else if(CNT(i*4+3 downto i*4)="0000") then
CNT(i*4+3 downto i*4)<="1001";elsif(((i>0)and(cnt((i-1)*4+3
downto (i-1)*4)="1001"))or(i=0))then CNT(i*4+3 downto
i*4)<=CNT(i*4+3 downto i*4)-1;end if;end if;end if;end
process;end generate;end BEHAV;
```

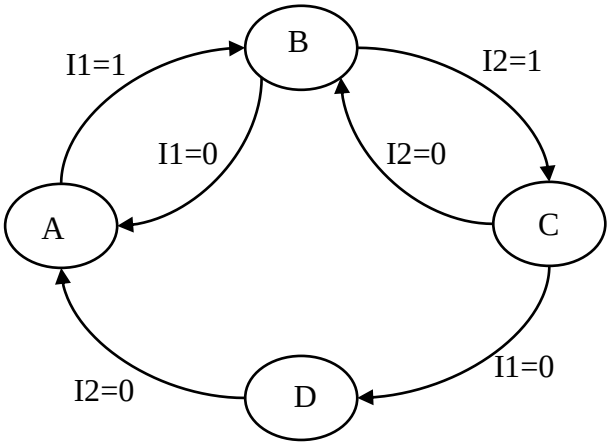
Note : Books, notes, computers are allowed in exam. 1 hour (sixty minutes)

2. The following block diagram is given. Each sub-block is a sub-circuit as a component. Design the top-level circuit using VHDL.




```
entity TopLevel is
...
```

3. The following state diagram and state-to-output-map are given. Design the circuit using VHDL.



A	100
B	110
C	101
D	011