No : Answer **Name : Solution**
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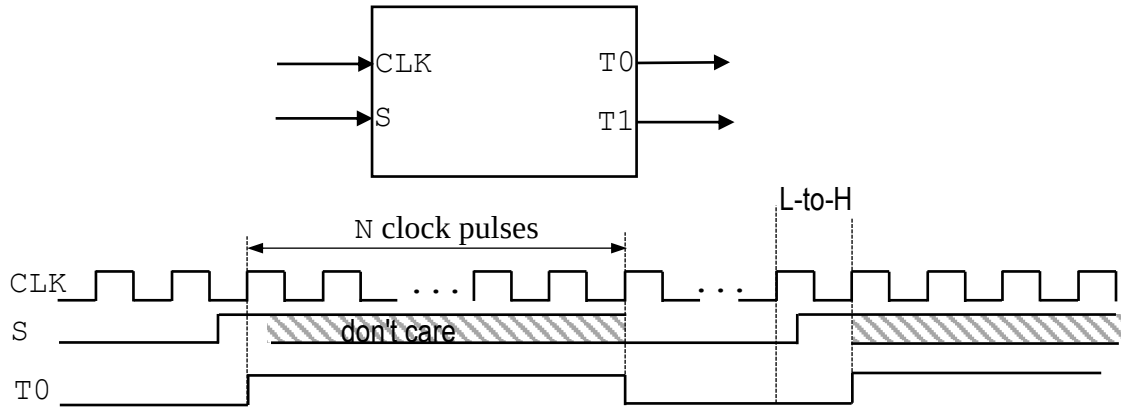
Department of Electrical Engineering & Electronics
"*Introduction To VHDL-FPGA*" Final Exam. 19.01.2021

A Timer/Counter is to be designed using VHDL. Block and timing diagram of the component is given;



Timing diagram shows the relation between `CLK`, `S` and `T0`; 0 to 1 transition of `S` between two rising edges of the `CLK` is used to start timer when `T0` is low. `S` does not have any effect when `T0` is high. That is, once `T0` is high, it will stay high for `N` clock periods and go low afterwards (`N` is a generic parameter). During that time, `S` will not have any effect.
`T1` is identical but it works with `not(S)`.
Design the circuit using VHDL.

```
entity MyTimer is Generic (N : in integer);
  port( CLK, S : in  STD_LOGIC;
        T0, T1 : out STD_LOGIC);
end MyTimer;
architecture MyTimer of MyTimer is -- your design below
  signal T0x,T1x,Sp : STD_LOGIC :='0';
  signal c0,c1  : integer := 0; -- two counters for two timers
begin
  T0 <= T0x; T1 <= T1x;
  process(CLK,S,T0x,T1x,c0,c1) is begin
    if(RISING_EDGE(CLK)) then
      Sp <= S;
      if(Sp&S="01") then T0x <= '1'; end if;
      if(Sp&S="10") then T1x <= '1'; end if;
      if(T0x='1') then
        if(c0=N-1) then T0x <= '0'; c0 <= 0; -- end timer 0
        else c0 <= c0+1; end if;
      end if;
      if(T1x='1') then
        if(c1=N-1) then T1x <= '0'; c1 <= 0; -- end timer 1
        else c1 <= c1+1; end if;
      end if;
    end if;
  end process;
end MyTimer;
```

Duration for this question : thirty (40) minutes