No : Answers **Name : Solutions**
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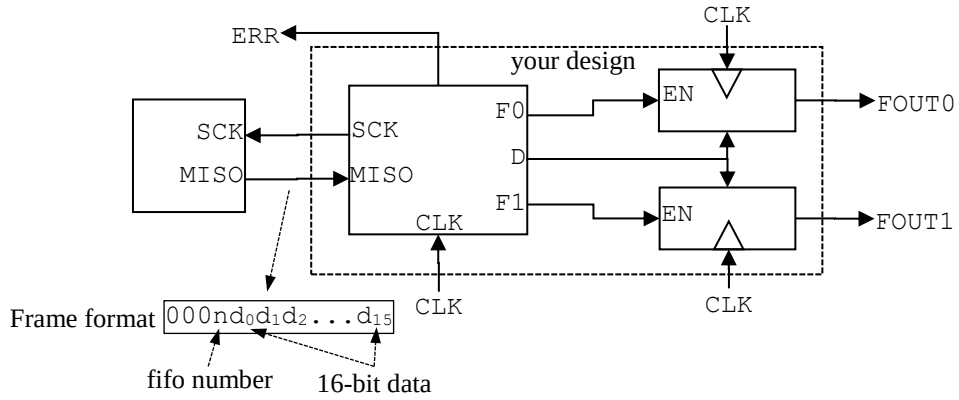
Department of Electrical Engineering & Electronics
"*Introduction To VHDL-FPGA*" Final Exam. 19.01.2021

An SPI slave sends data in frames of 20 bits on the falling edge of the clock provided by the SPI master (FPGA). First 3 bits are all 0 indicating frame-start, the next bit is the destination FIFO identifier. Master is to route the remaining 16 bits to identified FIFO buffer. If the first 3 bits are other than "000" the receiver generates an error indicator.




```
entity SPREC is Port (
  CLK, MISO : in STD_LOGIC;
  SCK, ERR, FOUT0, FOUT1 : out STD_LOGIC);
end SPREC;
architecture SPREC of SPREC is
  component FIFO is Port (
    CLK, EN, D : in STD_LOGIC;
    FOUT : out STD_LOGIC);
  end component;
-- your design below --
  signal cntr  : integer range 0 to 19;
  signal F0,F1 : STD_LOGIC;
begin
  SCK <= CLK;
  process(CLK,MISO,cntr) is begin
    if(RISING_EDGE(CLK)) then
      if(cntr<3) then
        F0 <= '0'; F1 <= '0'; -- FIFOs are disabled
        if(MISO='1') then ERR<='1'; end if;
      end if;
      if(cntr=3) then - FIFO selection
        if(MISO='0') then F0 <= '1';
        else F1 <= '1'; end if;
      end if;
      if(cntr=19) then cntr <= 0;
      else cntr <= cntr+1; end if;
    end if;
  end process;

  F0_inst: FIFO port map (CLK=>CLK, EN=>F0, D=>MISO, FOUT=>FOUT0);
  F1_inst: FIFO port map (CLK=>CLK, EN=>F1, D=>MISO, FOUT=>FOUT0);
end SPREC;
-- when REGs are used instead of FIFOs, MSB of REGs will be output
```

Duration for this question : thirty (30) minutes