No : Answers **Name : Solutions**
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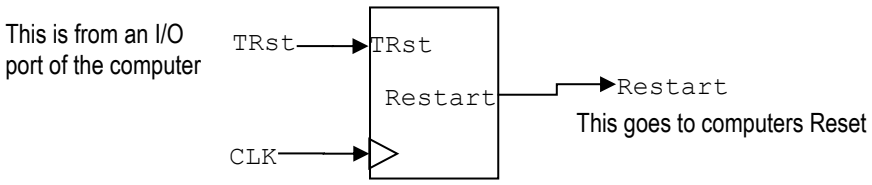
"*Introduction To VHDL-FPGA*" Final Exam. 19.01.2021

A watchdog timer is a hardware counter periodically reset by software. If it is not reset within the expected time-out period (meaning that the software is crashed) it will restart the software system.



For our particular implementation, assume that CLK is 50MHz and Restart stays high for 10 clock periods at the end of the time-out period. Time-out period is 2 sn. After `Restart`, timer waits for the first `TRst` rising edge, to be activated again. Design the watchdog timer in VHDL.
note: You may tweak the numbers for easier designs. For example, Time-out period can be 1.9 sn if it is easier for you.

```
entity WATCHDOG is Port (
  CLK, TRst : in STD_LOGIC;
  Restart : out STD_LOGIC);
end WATCHDOG;
architecture WATCHDOG of WATCHDOG is  -- your design below --
  signal cntr : integer range 0 to 100000000; -- 2 sn
  signal pTRst : STD_LOGIC :='0';
begin
  process(CLK,TRst,Rstrt) is begin
    if(RISING_EDGE(CLK)) then
      pTRst <= TRst;
      if(pTRst&TRst="01") then -- TRst has risen
        cntr <= 0; Restart <= '0';
      else
        if(cntr=99999990) then -- raise Restart 10 clk before 2 seconds
          Restart <= '1';
        end if;
        if(cntr=100000000) then -- lower Restart so that computer can start
          Restart <= '0';
        else
          cntr <= cntr+1;
        end if;
      end if;
    end if;
  end process;
end WATCHDOG;
```

Duration for this question : thirty (30) minutes