No : Answers **Name : Solutions**

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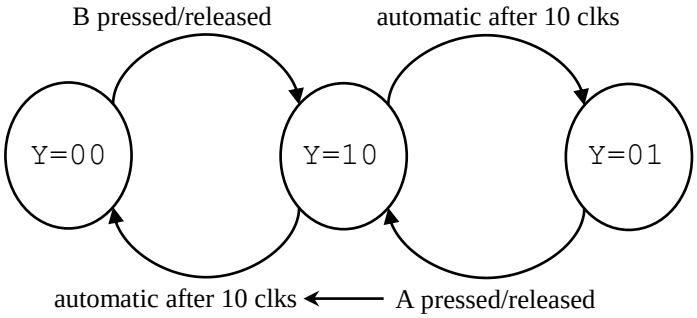
"*Introduction To VHDL-FPGA*" Midterm

Note : Books, notes, computers are allowed, communication of all kind is prohibited. 90 minutes.

1. A controller has two button inputs named as A and B, and one two-bits output named as Y. A and B buttons activate Y(1) and Y(0) bits with some transition period as explained in the following;
   a) When Y=00, pressing (and releasing) button B: Y becomes 10 immediately and becomes 01 after 10 clk periods. All inputs are ignored during this transition.
   b) When Y=01, pressing (and releasing) button A: Y becomes 10 immediately and becomes 00 after 10 clk periods. All inputs are ignored during this transition.



Design the controller using VHDL. Assume that the button signals are de-bounced.

```
entity CONTROLLER is Port (
    CLK  :    in STD_LOGIC;
    A, B :    in STD_LOGIC;
       Y : inout STD_LOGIC_VECTOR(1 downto 0));
end CONTROLLER;
architecture CONTROLLER of CONTROLLER is
  signal cntr  : integer;
  signal Ap,Bp : STD_LOGIC;
  signal X : STD_LOGIC_VECTOR(1 downto 0);
begin
  process(CLK,A,B,Y,cntr) is
  begin
    if(rising_edge(CLK)) then
      Ap <= A; Bp <= B;
      if(Y="10") then
        if(cntr=10) then Y <= X;
        else cntr <= cntr+1;
        end if;
      else
        if(Ap&A="01") then
          X <= "01"; Y <= "10";
        elsif(Bp&B="01") then
          X <= "00"; Y <= "10";
        end if;
        cntr <= 0;
      end if;
    end if;
  end process;
end CONTROLLER;
```

An interesting and efficient solution would be

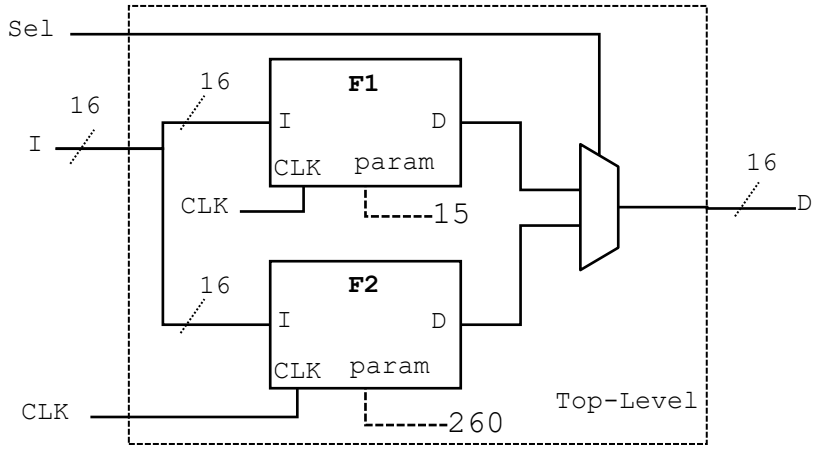
```
signal cntr : integer;
signal T : STD_LOGIC;
...
process...
  if((Y(0)='0')and((A or B)/='0')) then
    cntr <= 10;
    Y <= "10";
    T <= B;
  elsif((Y="10")and(cntr=0)) then
    Y <= '0' & T;
  end if;
  if(cntr/=0) then
    cntr <= cntr-1;
  end if;
```

2. Design a GENERIC clock divider. The generic parameter is the divisor and can be an integer from 2 to 255. The difference between on and off duty cycles of the generated lower freq. clock should be 1 input clock period at most. For example, if the input clock signal is 50 MHz and the generic parameter is 2 then the output clock signal frequency should be 25 MHz with 1 clock periods for both duty–cycles. If the divisor parameter is 3 then the duty-cycles should be 1 and 2 input clock periods respectively, making the output frequency 16666666.66... MHz.

```
entity CDIV is
  Generic (DV : in integer);
  Port (
    CLK  : in  STD_LOGIC;
    CLKO : out STD_LOGIC);
end CDIV;
architecture CDIV of CDIV is
  signal cntr : integer;
begin
  process(CLK) is begin
    if(rising_edge(CLK)) then
      if(cntr=DV) then
        CLKO <= '0';
        cntr <= 0;
      else
        if(cntr=DV/2) then
          CLKO <= '1';
        end if;
        cntr <= cntr+1;
      end if;
    end if;
  end process;

end CDIV;
```

3. The following partial code and a block diagram are given. Complete the top-level circuit using VHDL.




```
entity TOP is Port (
  CLK,Sel : in  STD_LOGIC;
        I : in  STD_LOGIC_VECTOR(15 downto 0);
        D : out STD_LOGIC_VECTOR(15 downto 0));
end TOP;
architecture TOP of TOP is
  component SUB is
   Generic(param : in integer);
   Port(
    CLK : in STD_LOGIC;
    I   : in STD_LOGIC_VECTOR(15 downto 0);
    D   : out STD_LOGIC_VECTOR(15 downto 0));
  end component;
  signal D1,D2: STD_LOGIC_VECTOR(15 downto 0);
begin
  F1:SUB Generic Map (param=>15);
    Port Map (CLK=>CLK, I=>I, D=>D1);
  F2:SUB Generic Map (param=>260);
    Port Map (CLK=>CLK, I=>I, D=>D2);
  D<=D1 when Sel='1' else D2;
end TOP;
```