No : Answers **Name : Solutions**

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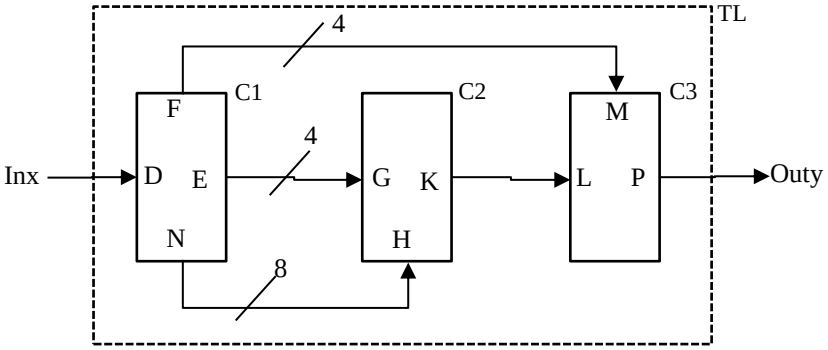
"*Introduction To VHDL-FPGA*" Midterm

Note : Books, notes, computers are allowed, communication of all kind is prohibited. 90 minutes.

1. A ready-to-use tone generator is given to be used in a 4 button circuit. Each button, when pressed, will generate a different tone for 1 seconds and send it to output.

```
entity Buttons is port (
  CLK : in  STD_LOGIC;   -- 50 MHz
  Btn : in  STD_LOGIC_VECTOR(3 downto 0);
  Tne : out STD_LOGIC);  -- to buzzer
end Buttons;
architecture Buttons of Buttons is
  component TGen is port (
    CLK : in  STD_LOGIC;  -- 50 MHz
    FRQ : in  STD_LOGIC_VECTOR(3 downto 0); -- tone select
    EN  : in  STD_LOGIC;   -- Enable
    TNE : out STD_LOGIC);  -- tone output
  end component;
  signal EN : STD_LOGIC;
  signal Btnp : STD_LOGIC_VECTOR(3 downto 0);
  signal cntr: integer range 0 to 50000000;
begin
  TG: TGen port map (
    CLK => CLK,
    FRQ => Btnp,
    EN  => EN,
    TNE => Tne
  );
  process(CLK) is begin
    if(rising_edge(CLK)) then
      Btnp <= Btn;
      if((Btnp/=Btn)or(EN='1')) then
        if(cntr<50000000) then
          cntr <= cntr+1; EN <= '1';
        else
          cntr <= 0; EN <= '0';
        end if;
      end if;
    end if;
  end process;
end Buttons;
```

2. Complete the following top-level circuit in VHDL.




```
entity TL is port (
  clk   : in  STD_LOGIC; -- 10 MHz
  Inx   : in  STD_LOGIC_VECTOR(3 downto 0);
  Outy  : out STD_LOGIC_VECTOR(3 downto 0));
end TL;
architecture TL of TL is
  component C1 is port(
    clk : in  STD_LOGIC; -- 10 MHz
    D   : in  STD_LOGIC_VECTOR(3 downto 0);
    E   : out STD_LOGIC_VECTOR(3 downto 0);
    F   : out STD_LOGIC_VECTOR(3 downto 0);
    N   : out STD_LOGIC_VECTOR(7 downto 0));
  end component;
  component C2 is port(
    clk : in  STD_LOGIC; -- 10 MHz
    G   : in  STD_LOGIC_VECTOR(3 downto 0);
    H   : in  STD_LOGIC_VECTOR(7 downto 0);
    K   : out STD_LOGIC_VECTOR(3 downto 0));
  end component;
  component C3 is port(
    L   : in  STD_LOGIC_VECTOR(3 downto 0);
    M   : in  STD_LOGIC_VECTOR(3 downto 0);
    P   : out STD_LOGIC_VECTOR(3 downto 0));
  end component;
  signal Ex, Fx, Kx : STD_LOGIC_VECTOR(3 downto 0);
  signal Nx : STD_LOGIC_VECTOR(7 downto 0);
begin
  C1i: C1 port map (clk=>clk,D=>Inx,E=>Ex,F=>Fx,N=>Nx);
  C2i: C2 port map (clk=>clk,G=>Ex,H=>Nx,K=>Kx);
  C3i: C3 port map (L=>Kx,M=>Fx,P=>Outy);
end;
```

3. A keyless entry circuit employs the following cipher-check sub-circuit CC. CC reads BCD input when EN is High and stores it to a local 4x4 memory (4 registers of 4-bits each). It outputs OK (active-high) signal when the entered 4 digit number is correct (same with the local constant 4 digit number) and keeps it High until Rst is High. Design the circuit in VHDL.

```
entity CC is port (
  clk : in  STD_LOGIC;
  Rst : in  STD_LOGIC;
  EN  : in  STD_LOGIC; -- High for 1 clk cycle on every BCD input
  BCD : in  STD_LOGIC_VECTOR(3 downto 0);
  OK  : out STD_LOGIC  -- normally Low. High when activated
);
end CC;
architecture CC of CC is
  constant Ndig: integer :=4;
  type M4 is array (0 to Ndig-1) of STD_LOGIC_VECTOR(3 downto 0);
  constant CL : M4 := (x"1",x"2",x"3",x"4");
  signal ML : M4:=(others=>x"F");
begin
  BR:process(clk) is begin
    if(rising_edge(clk)) then
      if(Rst='1') then
        OK <= '0';
        ML <=(others=>x"F");
      else
        if(EN='1') then
          ML(3) <= ML(2); -- or ML <= BCD & ML(0 to 2);
          ML(2) <= ML(1);
          ML(1) <= ML(0);
          ML(0) <= BCD;
        end if;
        if(ML=CL) then
          OK <= '1';
        end if;
      end if;
    end if;
  end process;
end CC;
```