No : Answers **Name : Solutions**
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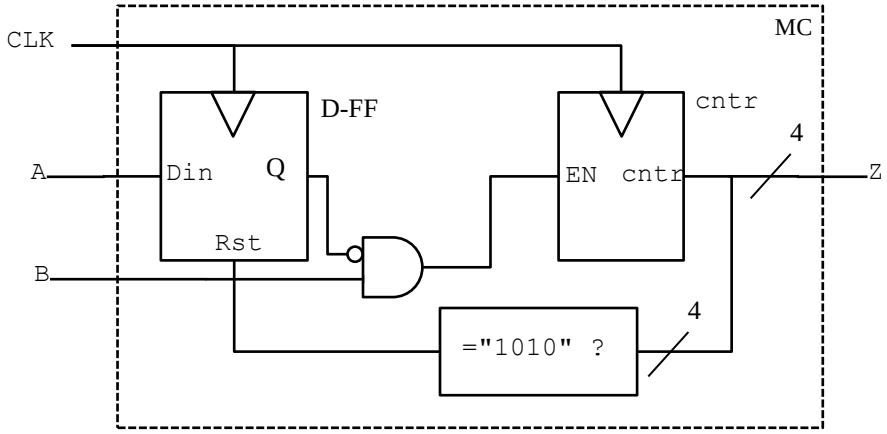
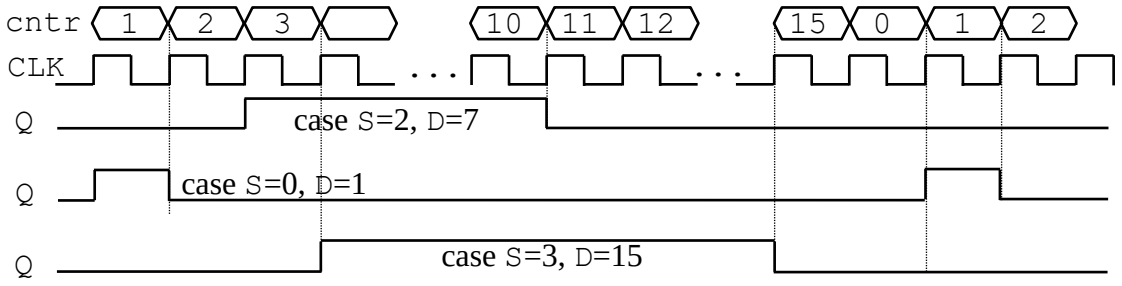
"*Introduction To VHDL-FPGA*" Midterm
Note : Books, notes, computers are allowed, communication of all kind is prohibited. 90 minutes.

1. Design the following circuit in VHDL within one process. `Rst` of D-FF is synchronous.



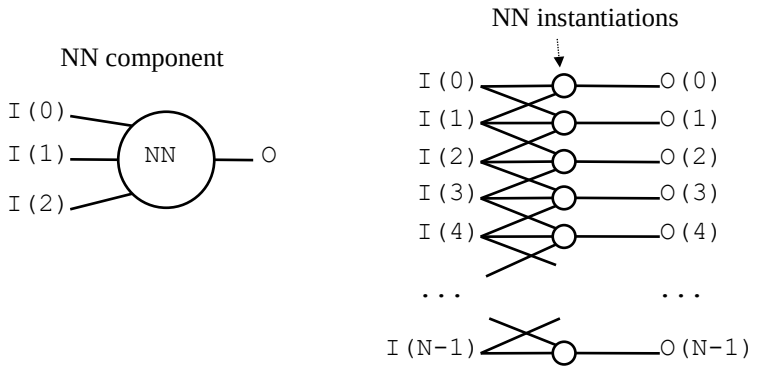

```
entity MC is port (
  clk, A, B : in STD_LOGIC;
  Z : out STD_LOGIC_VECTOR(3 downto 0));
end MC;
architecture MC of MC is
  signal cntr : STD_LOGIC_VECTOR(3 downto 0);
  signal Q : STD_LOGIC;
begin
  process(CLK) is begin
    if(rising_edge(CLK)) then
      if(cntr="10101") then
        Q <= '0';
      else
        Q <= A;
      end if;
      if((B='1')and(Q='0')) then
        cntr <= cntr+1;
      end if;
    end if;
    Z < cntr;
  end process;
end MC;
```

2. A counter counts from 0 to 15, incrementing 1 on every rising edge of CLK and going back to zero afterwards, continuously. Two inputs, start-time S and duration D, determine the rise and fall times of the output Q as exemplified below. Q goes to zero when counter is 14 regardless of D. Ranges for S and D are both (0,15), therefore for some cases of S & D, Q may not become '1' for entire cycle. Complete this circuit in VHDL.




```
entity PW is port (
  clk  : in  STD_LOGIC;
  S, D : in  integer range 0 to 15;
  Q    : out STD_LOGIC);
end PW;
architecture PW of PW is
  signal cntr : integer range 0 to 15;
begin
  process(CLK) is begin
    if(rising_edge(CLK)) then
      cntr <= cntr +1;
      if(cntr=14) then
        Q <= '0';
      elsif(cntr=S) then
        Q <= '1';
      elsif(cntr=S+D+1) then
        Q <= '0';
      end if;
    end if;
  end process;
end PW;
```

3. A 3-input 1-output component is given as illustrated by a block. Multiple instantiations of the component are used to construct a network as also shown. Unused inputs of the NN instantiations are connected to '0'. The number of instantiations are given as a generic parameter `N`.




```
entity NNS is generic (N : integer:=100);
  port ( clk : in  STD_LOGIC;
    I : in  STD_LOGIC_VECTOR(0 to N-1);
    O : out STD_LOGIC_VECTOR(0 to N-1)
  );
end NNS;
architecture NNS of NNS is
  component NN is
    port (clk : in  STD_LOGIC;
      I : in  STD_LOGIC_VECTOR(0 to 2);
      O : out STD_LOGIC);
  end component;
  signal Ix: STD_LOGIC_VECTOR(-1 to N);
begin

  Ix(0 to N-1) <= I; Ix(-1)<='0'; Ix(N)<='0';

  L1:for i in 0 to N-1 generate
    inst: NN port map (
      CLK => CLK,
      I => Ix(i-1 to i+1),
      O => O(i)
    );
  end generate;

end NNS;
```